

FIG. 1 (Prior Art)

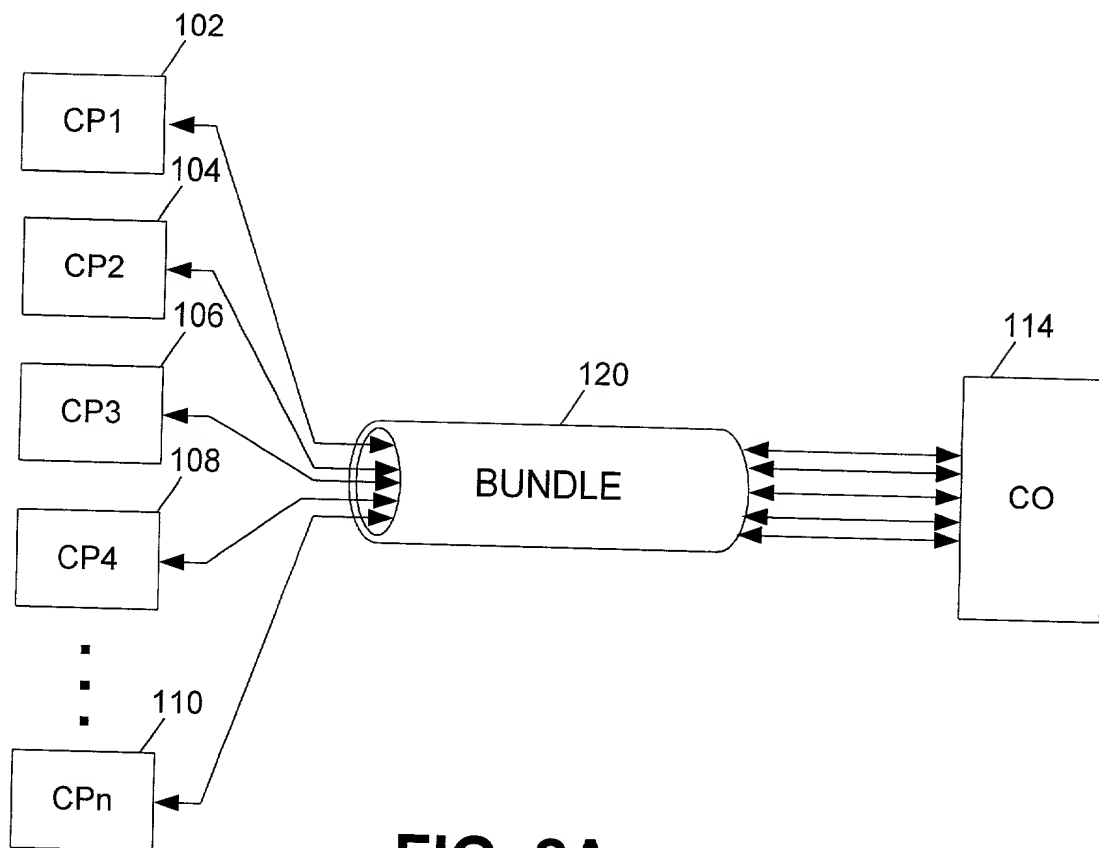


FIG. 2A

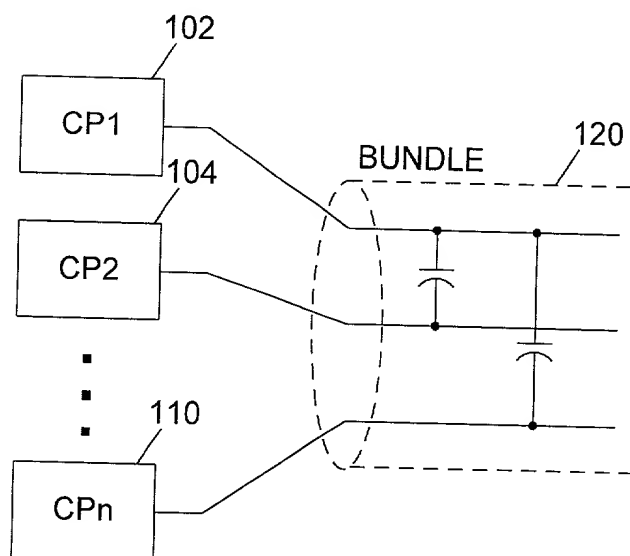


FIG. 2B

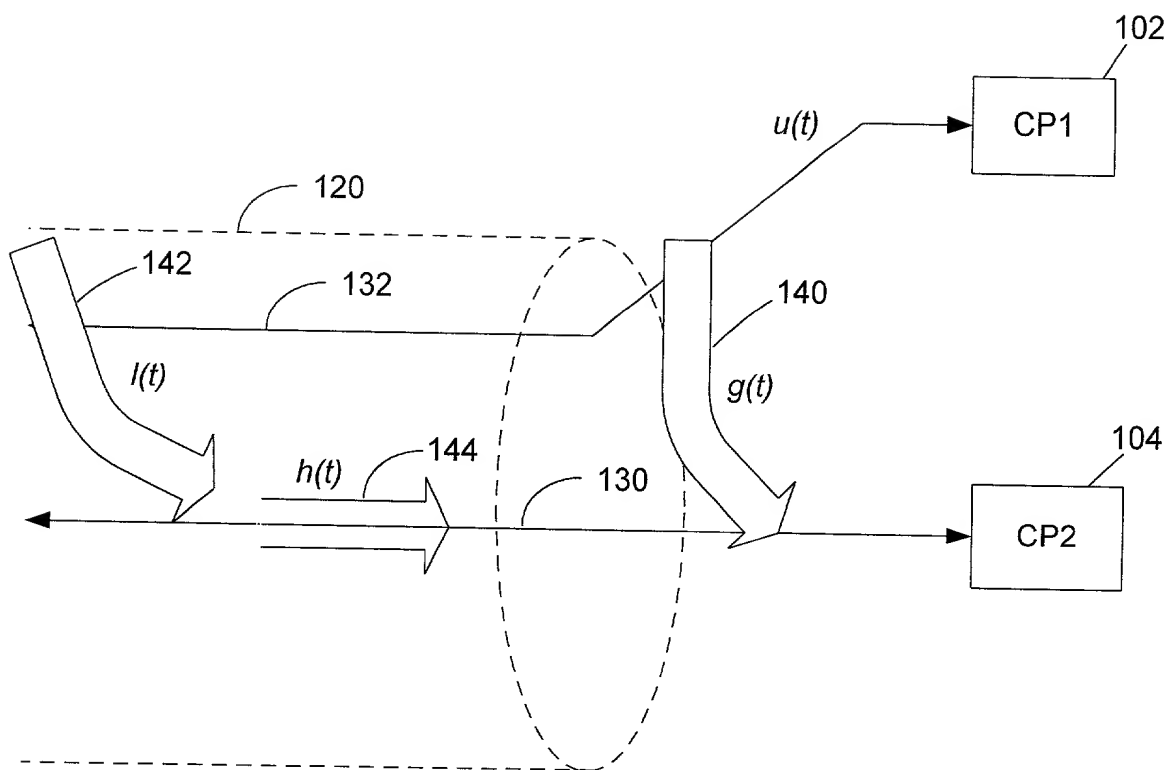


FIG. 3A

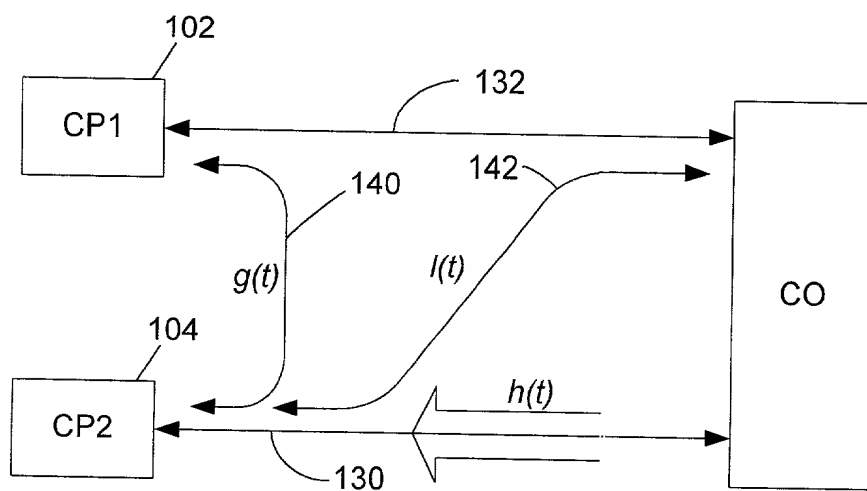


FIG. 3B

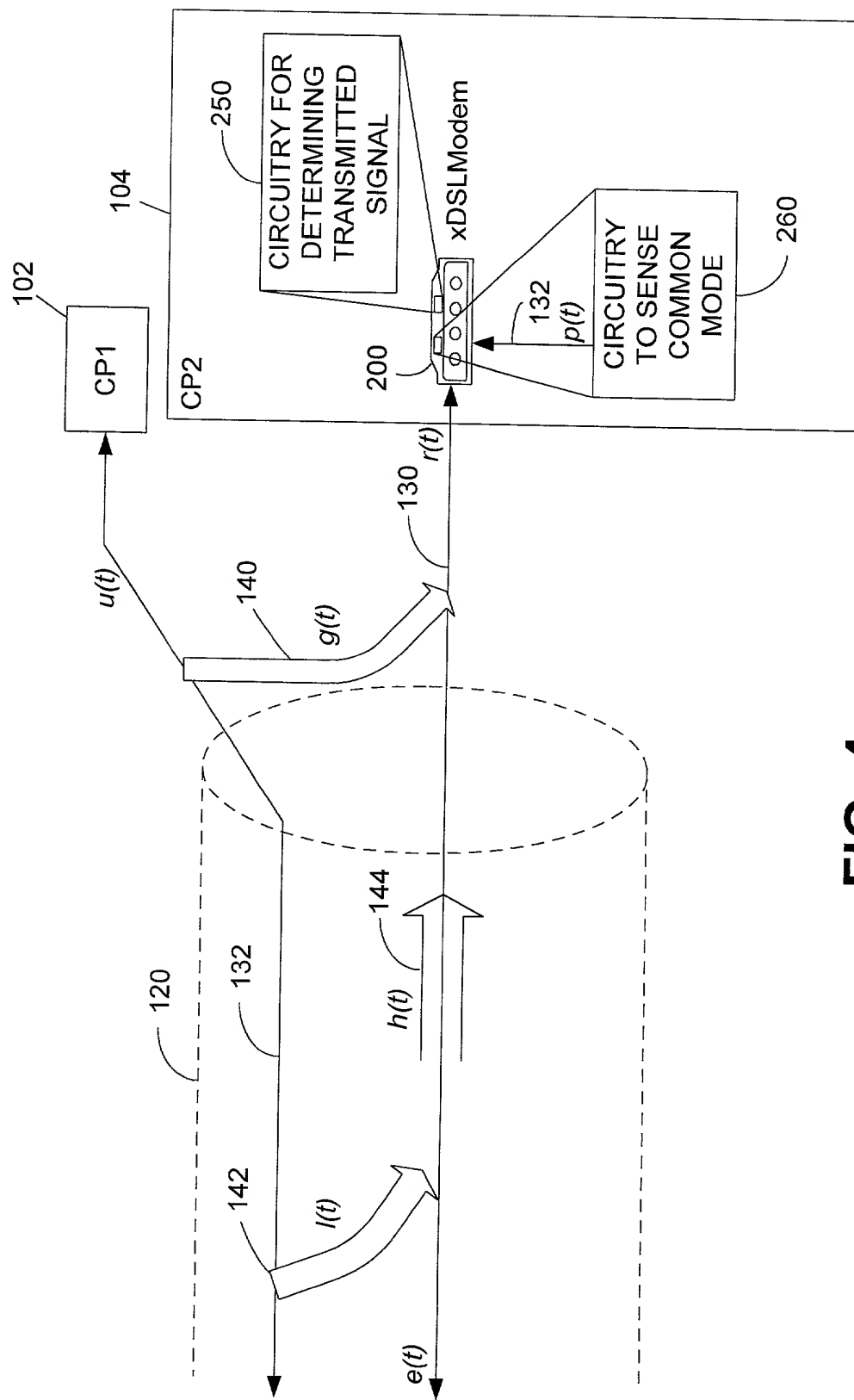


FIG. 4

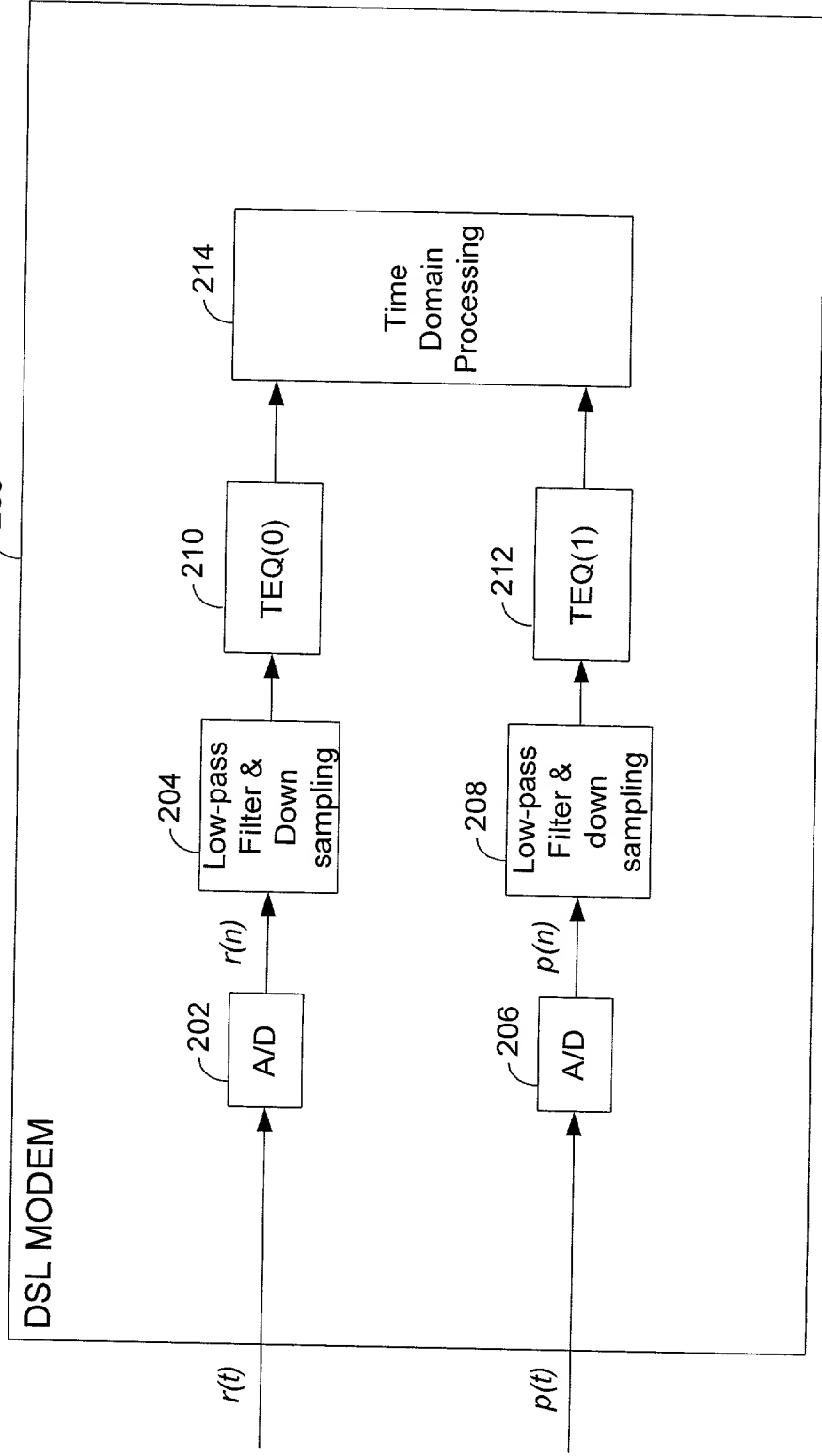


FIG. 5

FIG. 6 is a block diagram of a modem receiver 300. The receiver 300 includes two parallel processing paths for signals $r(t)$ and $p(t)$. Each path consists of an A/D converter (302, 306), a low-pass filter (304, 308), a TEQ block (310, 312), an FFT block (322, 324), and a frequency domain processing block (314). The outputs of the FFT blocks (322, 324) are fed into the frequency domain processing block (314).

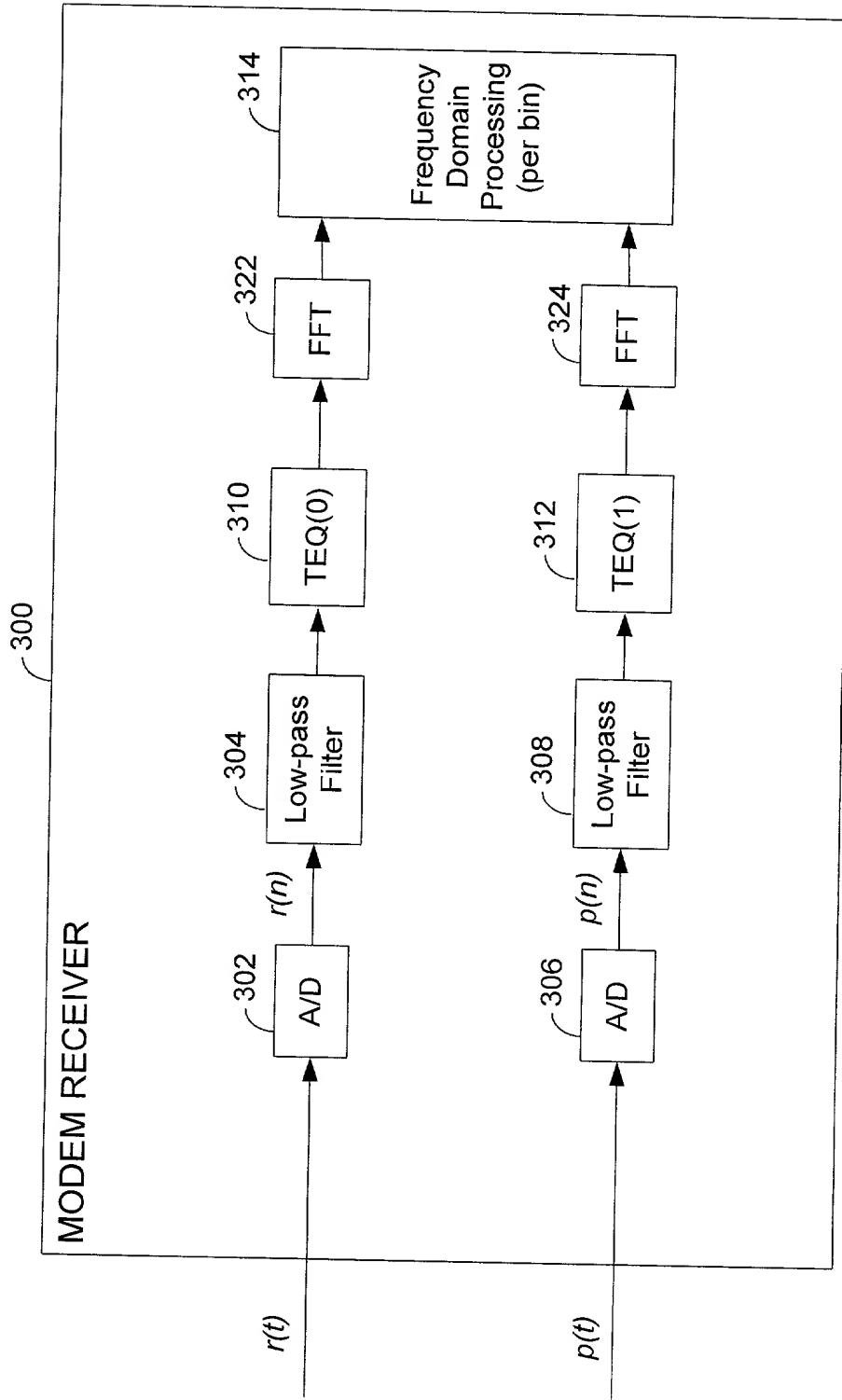


FIG. 6

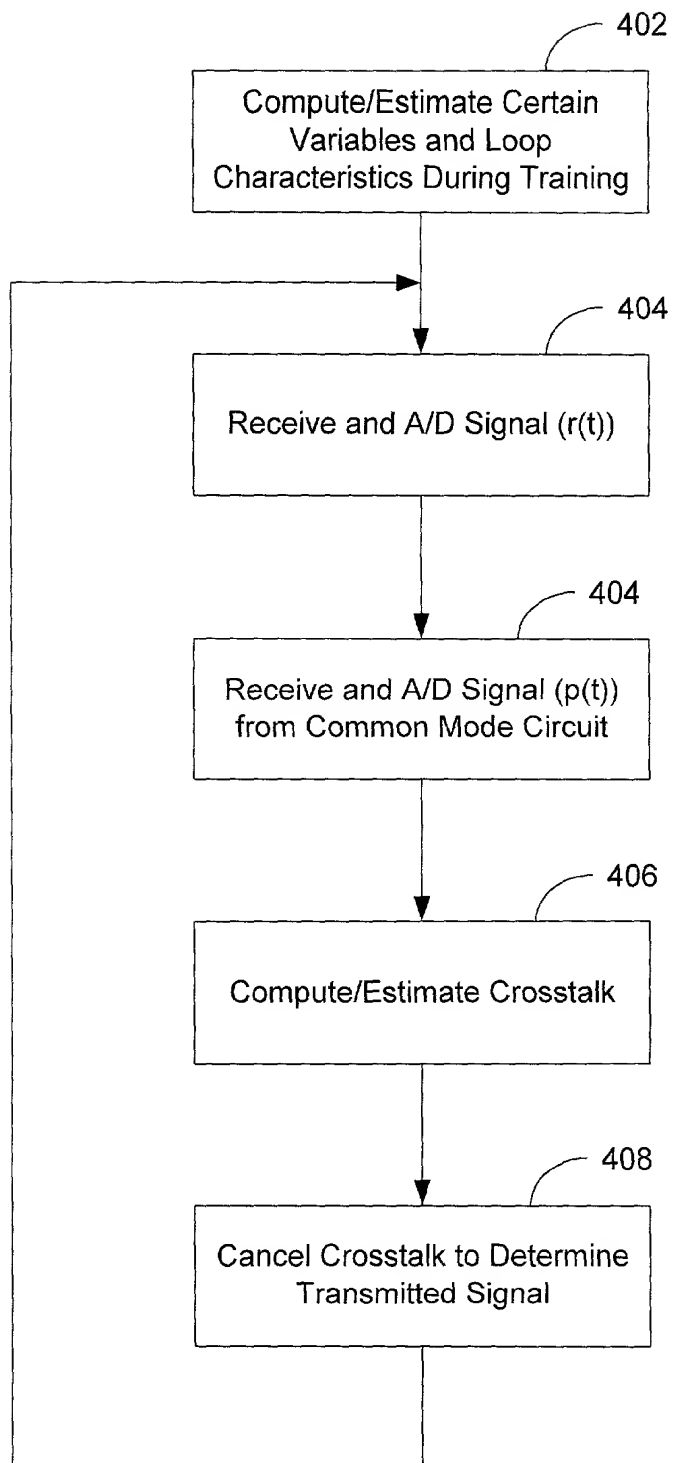


FIG. 7

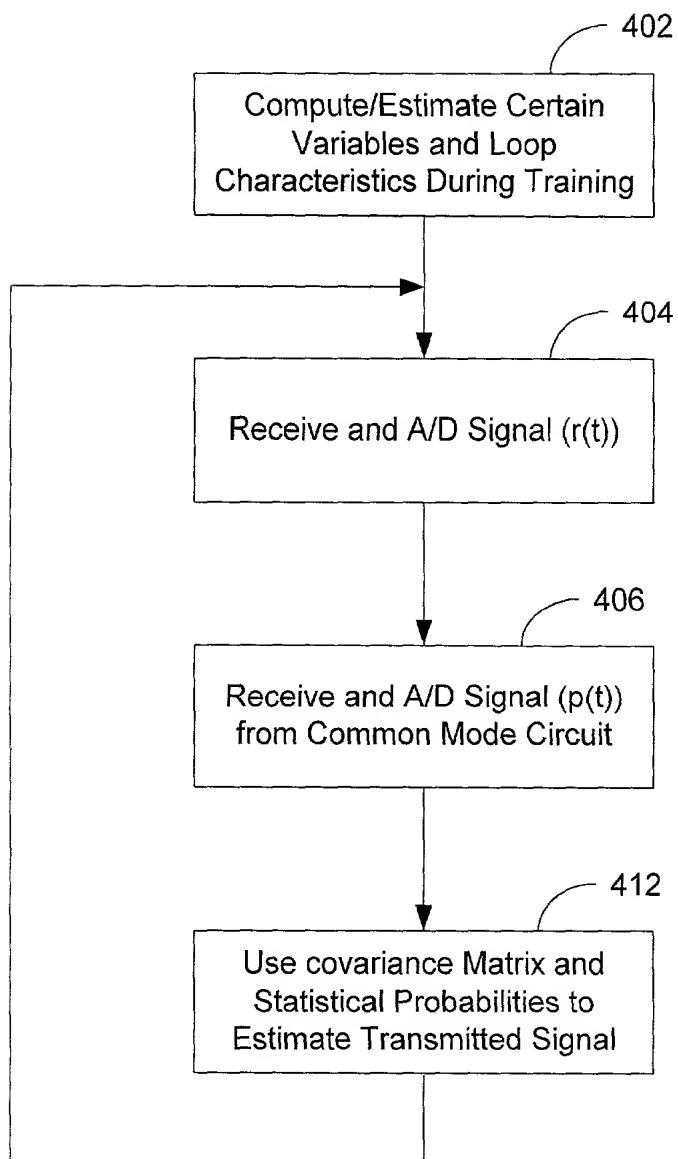


FIG. 8

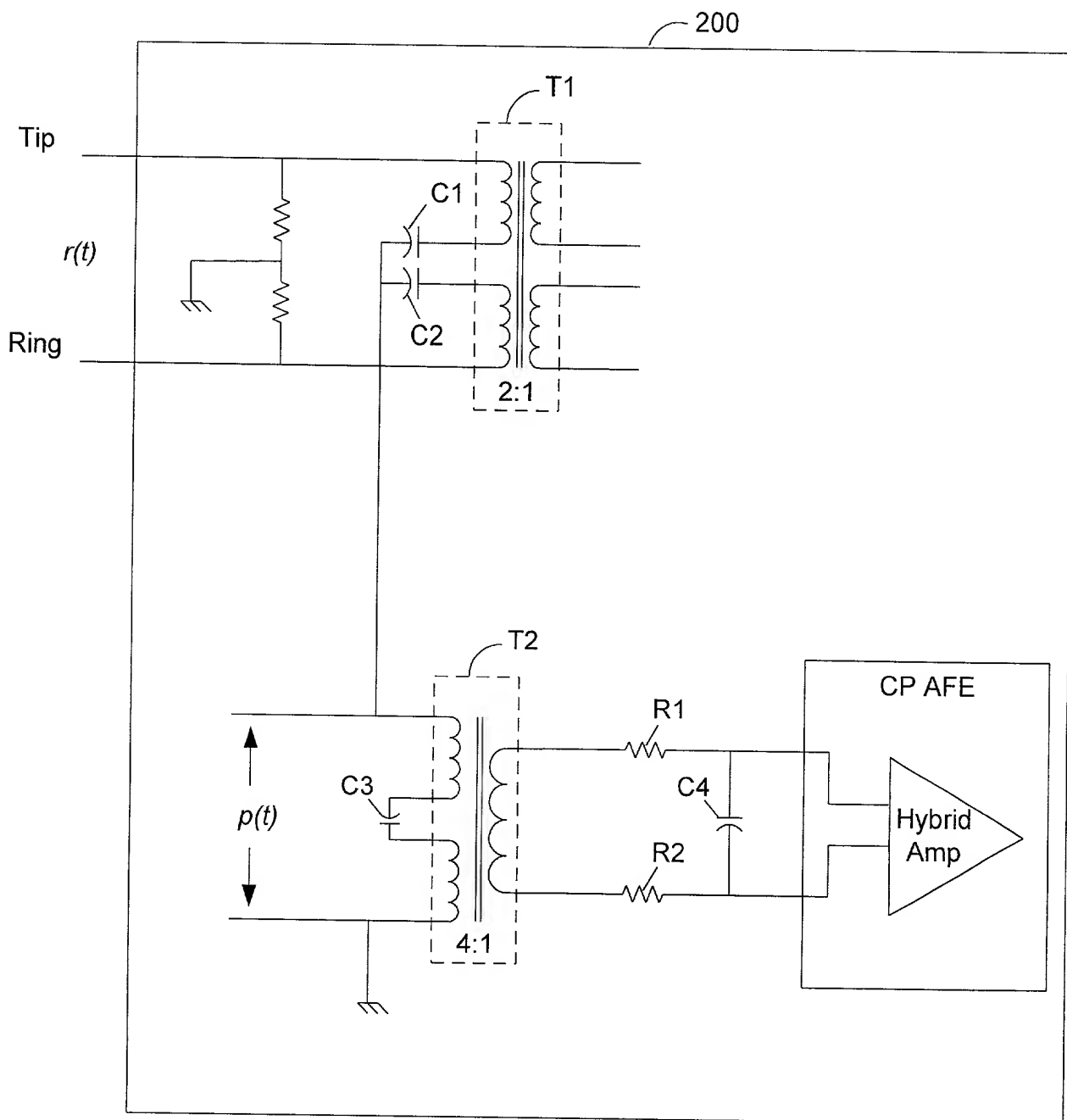


FIG. 9